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QUESTION BANK (DESCRIPTIVE)

Subject with Code : COA (16EC408) **Course & Branch**: B.Tech – ECE

Year & Sem: II-B.Tech & II-Sem **Regulation:** R16

UNIT –I

Introduction to Computer Organization and Architecture

1. a) Explain the basic components of Generic Computing system regardless of its internal architecture with practical real time examples [6M]
   b) Explain the phases involved in Instruction cycle with the help of necessary timing diagrams? [6M]
2. a) Sketch the internal organization of CPU out with its functionalities and block diagram. [8M]
   b) Write about hierarchy of buses, bus signals and its functionalities. [4M]

3. a) Elaborate how CPU is concordant with its Input & Output devices and explain the interfacing modules involved? [6M]
   b) Demonstrate how the Compatibility between CPU & Bidirectional IO components are devised using its interfacing modules [6M]

4. a) Imagine you are storing a video game in your computer and you want to play it now. With this assumption answer the following questions
   i. In which type of memory reserved bootable information resides and why? [2M]
   ii. Which memory component contains your video game and why? [2M]
   iii. Once you click on the video game, where will it be loaded and why? [2M]
   iv. Mostly Hard disk is preferred as secondary storage device rather than SRAM. Justify it. [2M]

   b) Construct and explain the 2-dimensional organization of 8x2 ROM chip? [4M]

5. a) List out the features of different levels in computer programming languages? [6M]
   b) Explain about compiling process and assembly process with a neat flow diagram? [6M]

6. a) List out the general aspects of ROM, RAM and IO interfacing modules. [4M]
   b) Design a relatively simple computer which incorporates 8K RAM, 8K ROM, IO interfacing modules along with processor. [8M]

7. a) With suitable paradigms, describe the Instruction types used in Assembly level languages. [6M]

   b) Elucidate modes of addressing used in assembly language instructions with examples? [6M]

8. a) Identify the crucial features to design the instruction set architecture for a specific purpose processor? [6M]
   b) Describe the Instruction set Architecture of simple computer. [6M]

9. a) Explain Linear organization of an 8*2 ROM chip with diagram? [4M]
   b) Justify importance of Backward Compatibility in Processor design with practical examples. [4M]
   c) Differentiate SRAM and DRAM. [4M]

10. a) Differentiate High level and low level langauges. [3M]
    b) What is an Interrupt? [3M]
    c) Draw block diagram for a bidirectional input/output device with its interface and enable/load logic? [3M]
    d) Design an 8x4 memory subsystem constructed from two 8x2 ROM chips? [3M]

UNIT –II

CPU Design and Computer Arithmetic

1. a) What is an instruction cycle and write the phases of Instruction cycle? [3M]
   b) With a neat flowchart, explain how the control unit determines the instruction after decoding an instruction. [9M]
2. a) Write the basic instruction formats for IO, Register and Memory Reference instructions. [3M]

   b) With a neat schematic, explain the steps involved in fetch and decode phases using register transfer instructions. [9M]

3. a) Elaborate the steps involved in execution of Memory-Reference instructions with its timing signals [4M]
   b) Using the register transfer notations, explain the Memory-Reference instructions with examples. [8M]
4. a) Illustrate the basic requirements for Input and Output communication using a terminal unit such as keyboard and printer. [8M]

   b) Tabulate the Input-Output Instructions using register transfer notations? [4M]

5. a) Write about Interrupt and its types? [6M]
   b) Illustrate the phases of Interrupt Cycle with a neat flowchart. [6M]

6. a) Design hardware for signed magnitude addition and subtraction? [6M]
   b) Explain the process for signed magnitude addition and subtraction with flow chart. [6M]

7. a) Implement hardware for multiplying Two fixed- point binary numbers in signed-magnitude representation along with its flowchart. [3M]

   b) Explain in detail about booth multiplication algorithm with an example? [9M]

8. a) Describe the importance of BCD in digital system design. [6M]
   b) Design a Decimal Arithmetic Unit to perform BCD addition and BCD Subtraction. [6M]

9. a) Tabulate data transfer instructions with examples in detail? [6M]
   b) Tabulate data manipulation instructions with examples in detail? [6M]

10. a) What is the use of program control instructions? Mention its typical instructions? [6M]
    b) Explain in detail about status bit conditions with example? [6M]

UNIT –III

Register Transfer Language and Design of Control unit

1.a) Why RTL is preferred for describing internal organization of digital computers. [2M]

b) Illustrate the register transfer mechanism for P: R2← R1 with necessary diagrams. [8M]

2. a) Design Bus system for Four-bit register using 4x1 Mux. [6M]
b) Implement Bus line for an 8-bit register using three state-buffers. [6M]

3. a) List out the Register transfer notations for Arithmetic Micro Operations. [2M]
b) Design and implement 4-bit Arithmetic unit which performs ADD, ADD with carry, SUB, Sub with borrow, Increment and decrement operations. [10M]

4 a) Tabulate the logical and shift micro operations with its RTL notations. [4M]
b) Implement 4-bit Binary Adder-Subtractor and Binary Incrementor. [8M]

5. a) Explain the logical micro operations which manipulates individual bits of word in register with examples. [6M]
b) Implement a 4-bit combinational circuit shifter using Multiplexer. [6M]

6 a) Demonstrate the general configuration of Micro programmed Control unit with a neat block diagram. [4M]
b) Explain about address sequencing in control memory with neat diagrams? [8M]

7. Present a Simple digital computer and show how it can be micro programmed with the help of necessary formats and notations. [12M]

8. a) Illustrate the phases involved in decoding of micro operation fields with necessary diagrams. [6M]
b) Draw and explain the schematic of Micro program sequencer for a control memory. [6M]

9. a) What is the difference between a micro-processor and a micro program? Is it possible to design a microprocessor without a micro program? [4M]
b) Differentiate Hardwired and Micro programmed control unit. Is it possible to have a hardwired control associated with a control memory? [4M]
c) Define i. Micro operation ii. Microinstruction iii. Micro program [4M]

10.a) Design a 4-bit ALU which performs arithmetic, Logical and shift operations. [6M]
b) write about hardware organization of micro programmed control unit. [6M]

UNIT –IV

Memory and Input/Output Organization

1. a) Discuss the Memory Hierarchy in computer system with regard to Speed, Size and Cost? [6M]
   b) Explain about main memory and its types. [6M]

2. a) Write about Auxiliary memory devices. [3M]
   b) Explain the mechanism involved in Magnetic Disks and Magnetic Tapes. [9M]

3. a) Write a suitable practical scenario for Content Addressable memory? [2M]
   b) Brief out the hardware organization of Associative memory with diagrams. [10M]
4. a) What is Locality of Reference and explain about Cache memory in detail. [4M]
   b) Illustrate the mapping process involved in transformation of data from main to Cache memory. [8M]
5. a) What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping? [6M]
   b) Explain Virtual address Mapping using Pages with necessary examples. [6M]

6. a) List out the importance of interfacing. [2M]
   b) With practical Examples, Explain the connection of I/O bus to input-output devices and its mapping Specifications. [10M]

7. a) Explain in detail about strobe control method of asynchronous data transfer? [6M]
   b) What is the disadvantage of strobe method? Explain how handshake method solves the problem? [6M]

8. Classify and describe the possible modes of data transfer to and from peripherals with examples. [12M]

9. a) List out the methodologies involved in handling Priority Interrupt. [2M]
   b) Explain Daisy-Chaining priority and Parallel priority Interrupt with its hardware diagram. [10M]

10. a) Elaborate how DMA bypasses CPU and speeds up the memory operation? [4M]
    b) With a neat schematic, Explain about DMA controller and its mode of data transfer. [8M]

UNIT –V
Pipeline and Multiprocessors

1. a) Justify how parallel processing improves the performance of multiprocessing environment? [4M]

   b) Illustrate a processor with multiple functional units with a neat diagram. [4M]

   c) Classify organisation of computers using Flynn's criteria. [4M]

2. a) Write about pipelining and its importance in high speed applications. [4M]

   b) Demonstrate the pipeline organisation for following example $A_i*B_i+C_i$ for i =1,2,3,…… [8M]

3. a) Illustrate the behavior of a pipeline using space-time diagram. [8M]

   b) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six – segment pipeline with a clock of 10 ns. Determine speedup ratio of the pipeline for 100 tasks. [4M]

4. a) Implement a simple pipeline unit for floating addition and subtraction. [6M]

   b) Consider an adder circuit with delays of four segment as t_1=60 ns, t_2=70 ns,t_3=100 ns,t_4=80 ns and interface resistors have a delay of t_r=10 ns. [6M]

   i) Find the clock cycle for pipeline.

   ii) Find out clock cycle for non-pipelined adder.

   iii) Speed up of pipelined over non-pipelined.

5. a) With examples, Explain four segment CPU pipeline and Timing of instruction pipeline. [6M]

   b) Elaborate the major difficulties that cause the instruction pipeline to deviate from its normal operation. [6M]

6. a) Differentiate tightly coupled and loosely coupled multiprocessors. [4M]

   b) Write about Time shared common bus and multiport memory. [8M]

7. a) Write down the physical forms available for establishing an interconnection network. [3M]

   b) Explain in detail about crossbar switching, Multistage switching network and hypercube system. [9M]

8. a) Explain how to resolve multiple contentions in shared resources. [3M]

   b) Illustrate serial and parallel arbitration produces in a shared multiprocessor environment. [9M]

9. Explain inter processor communication and synchronization in a shared multiprocessor environment. [12M]

10. a) Implement a simple pipeline unit for floating addition and subtraction. [6M]

    b) With examples, Explain four segment CPU pipeline and Timing of instruction pipeline. [6M]

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